REMARKS

New Claim 24 is added. Claims 1-4, 7-8, 12-13, 16-21 and 23-24 are pending. Claims 1, 4, 7, 13, 16, 21 and 23 are amended herein. No new matter is added by the claim amendments. Support for the claim amendments can be found at least on page 11 (lines 6-15), page 12 (lines 2-4) and page 13 (lines 9-10).

Drawings

According to the instant Office Action, Figures 1 and 2 should be designated as "prior art" "because only that which is old is illustrated." Applicant respectfully requests that a basis be provided for the conclusion that Figures 1 and 2 only illustrate that which is old.

Also, the drawings are objected to because, according to the Office Action, they do not show an "emitter follower for the emitters of said plurality of transistor" (sic) and "a voltage pull up device." The "emitter follower" refers to element 309 of Figure 3, and the previously claimed "plurality of transistors" refers to elements 203, 204 and 205 of Figure 3. The "voltage pull up device" refers to element 320 of Figure 3. Accordingly, Applicant respectfully submits that the features at issue are shown in Figure 3.

Also, the drawings are objected to because Figure 3 fails to show any of the details or include a text label for element 320. The instant specification refers to "device 320," which is described as being implemented in a number of different ways, such as a resistor or transistor. According to 37 CFR § 1.83, conventional features (which presumably include a resistor or transistor) can be illustrated in the form of a labeled representation (e.g., a labeled rectangular box). Applicant respectfully submits that Figure 3 (specifically, device 320) satisfies this requirement. The Examiner argues

that element 320 should be labeled to facilitate patent searches and reviews. Applicant can find no such requirement in the rules and regulations that govern and guide the Patent Office. Nevertheless, Figure 3 is amended.

35 U.S.C. § 112 Rejections

According to the instant Office Action, Claims 1-4, 7-8, 12-13, 16-21 and 23 are rejected under 35 U.S.C. § 112, second paragraph. Claim 1, for example, previously recited "a band-gap reference unit comprising a plurality of transistors" (emphasis added). The Examiner is respectfully directed to MPEP § 2111.03, which states that the transitional term "comprising" "is synonymous with 'including,' ... is inclusive or open-ended and does not exclude additional, unrecited elements" (emphasis added). Applicant respectfully submits that the previously claimed "plurality of transistors" is improperly interpreted as including all of the transistors 201-207 of Figure 3. The use of the transitional term "comprising" means that the claimed "band-gap reference unit" includes transistors 203, 204 and 205 and may or may not include other elements. In other words, the previously claimed "plurality of transistors" rightfully refers to transistors 203, 204 and 205. Read as such, the claims would satisfy the requirements of 35 U.S.C. § 112, second paragraph. Regardless, the claims as amended herein satisfy the requirements of 35 U.S.C. § 112, second paragraph.

Also, Claims 7 and 16 are amended to address the lack of antecedent basis identified in the Office Action.

In addition, Claims 13 and 21 are amended as shown to address the issue raised in the Office Action.

35 U.S.C. § 102 Rejections

According to the instant Office Action, Claims 1-4, 7-8, 12-13 and 16-21 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kadanka et al. ("Kadanka;" U.S. Patent No. 5,920,184). The Applicant has reviewed the cited reference and respectfully submits that the present invention as recited in Claims 1-4, 7-8, 12-13 and 16-21 is neither anticipated nor rendered obvious by Kadanka.

According to the Federal Circuit, "[a]nticipation requires the disclosure in a single prior art reference of each claim under consideration" (W.L. Gore & Assocs. v. Garlock Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983)). However, it is not sufficient that the reference recites all the claimed elements. As stated by the Federal Circuit, the prior art reference must disclose each element of the claimed invention "arranged as in the claim" (emphases added; Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)).

Applicant respectfully submits that Kadanka does not show or suggest the claimed circuit structure or the claimed functionality of the circuit in operation. Specifically, Applicant respectfully submits that Kadanka does not show or suggest "a band-gap reference unit comprising a first transistor, a second transistor and a third transistor, wherein said first and second transistors share a common base that is shunted to the collector of said first transistor and wherein said third transistor is coupled to the collector of said second transistor; a buffer circuit ...; a voltage pull-up device ... implemented as a fourth transistor; and a fifth transistor operable as an emitter follower for the emitters of said first, second and third transistors, wherein the emitter of said fifth transistor is coupled to the base of said buffer circuit via said voltage pull-up device, the base of said fifth transistor is coupled to each of the emitters of said

first, second and third transistors, and the collector of said fifth transistor is coupled to Vcc; and wherein said fifth transistor and said voltage pull-up device in combination pull the V_{BE} of said buffer circuit toward Vcc" as recited in independent Claim 1 and as similarly recited in independent Claims 7 and 16.

Accordingly, Applicant respectfully submits that Claims 1, 7 and 16 are in condition for allowance. Claims 2-4, 8, 12-13 and 17-21 depend from either Claim 1, 7 or 16 and recite additional limitations. Consequently, Applicant respectfully submits that Claims 2-4, 8, 12-13 and 17-21 are also in condition for allowance because they each depend on an allowable base claim.

In summary, Applicant respectfully asserts that the basis for rejecting Claims 1-4, 7-8, 12-13 and 16-21 under 35 U.S.C. § 102(b) is traversed.

35 U.S.C. § 103 Rejections

According to the instant Office Action, Claim 23 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kadanka in view of Mietus (U.S. Patent No. 5,666,046). The Applicant has reviewed the cited references and respectfully submits that the present invention as recited in Claim 23 is neither anticipated nor rendered obvious by Kadanka and Mietus, either alone or in combination.

Claim 23 is dependent on Claim 16 and includes additional limitations. Hence, by demonstrating that Claim 16 is not shown or suggest by the combination of references cited, it is also demonstrated that Claim 23 is not shown or suggested by the combination of references.

As presented above, Applicant respectfully asserts that Claim 16 is not shown or suggested by Kadanka. Applicant respectfully submits that Mietus does not overcome the shortcomings of Kadanka. More specifically, Applicant respectfully submits that Mietus, alone or in combination with Kadanka, does not show or suggest "adjusting voltage across said buffer circuit, by use of a voltage pull-up device in combination with a fourth transistor to pull the V_{BE} of said buffer circuit toward Vcc, wherein said voltage pull-up device is coupled between said buffer circuit and said band gap voltage reference unit, so that said band-gap reference voltage is maintained, wherein said fourth transistor is coupled as an emitter follower for the emitters of said first, second and third transistors, wherein the emitter of said fourth transistor is coupled to the base of said buffer circuit via said voltage pull-up device, the base of said fourth transistor is coupled to each of the emitters of said first, second and third transistors, and the collector of said fourth transistor is coupled to Vcc" where "said first and second transistors share a common base that is shunted to the collector of said first transistor and wherein said third transistor is coupled to the collector of said second transistor" as recited in Claim 16. Applicant respectfully submits that Mietus, like Kadanka, does not show or suggest the claimed circuit structure or the claimed functionality of the circuit in operation as recited in Claim 16.

Accordingly, Applicant respectfully submits that Claim 16 is allowable over Kadanka and Mietus. Therefore, Applicant respectfully submits that Claim 23 is also in condition for allowance because it depends on an allowable base claim.

In summary, Applicant respectfully asserts that the basis for rejecting Claim 23 under 35 U.S.C. § 103(a) is traversed.

Conclusions

In light of the foregoing amendments and remarks, Applicant respectfully submits that Claims 1-4, 7-8, 12-13, 16-21 and 23-24 are in condition for allowance. Applicant respectfully requests allowance of the pending claims.

The Applicant has reviewed the references cited but not relied upon and did not find these references to show or suggest the present claimed invention: U.S. Patent Nos. 5,834,927, 5,602,466, 4,683,416, 4,422,033 and 3,886,001.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Respectfully submitted,

MURABITO HAO & BARNES LLP

Dated: 12/21, 2007

William A. Zarbis
Registration No.: 46,120

Two North Market Street
Third Floor
San Jose, CA 95113

(408) 938-9060

AMENDMENTS TO THE FIGURES

Figure 3 is amended to include a label for element 320. A replacement sheet for Figure 3 is provided with this response.